SIDDHARTHA
INSTITUTE OF TECHNOLOGY & SCIENCES
Korremula Road, Narapally, Ghatkesar Mandal, Ranga Reddy District.

LABORATORY MANUAL

For

ELECTRONIC CIRCUIT ANALYSIS

(II B. Tech ECE- II Semester- R18 .AY:2022 - 23)

Prepared by

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Department of

Electronics & Communication Engineering

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SIDDHARTHA INSTITUTE OF TECHNOLOGY & SCIENCES

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SIDDHARTHA INSTITUTE OF TECHNOLOGY & SCIENCES

VISION & MISSION OF THE INSTITUTE

VISION:

To be a Centre of Excellence in Technical Education and to become an epic center of Research for creative solutions.

MISSION:

To address the Emerging Needs through Quality Technical Education with an emphasis on practical skills and Advanced Research with social relevance.

OBJECTIVES:

- To translate our vision into action and accomplish our mission, we strive to provide state-of-art infrastructure.
- Recruit, Motivate and develop faculty of high caliber and with multiple specialization.
- Continuously review, innovate and experiment teaching methodologies and learning processes.
- Focus on research, training and consultancy through an Integrated Institute-Industry symbiosis.

SIDDHARTHA INSTITUTE OF TECHNOLOGY & SCIENCES

VISION & MISSION OF THE DEPARTMENT

VISION :

To provide innovative teaching and learning methodologies for excelling in a high-value career, higher education and research to the students in the field of Electronics and Communication Engineering to meet the needs of the industry and to be a part of the advancing technological revolution.

MISSION :

- To create engineers of high quality on par with international standards by providing excellent infrastructure and well qualified faculty.
- To establish centers of excellence to enhance collaborative and multidisciplinary activities to develop human and intellectual qualities.
- To provide technical expertise to carry out research and development.

PROGRAM EDUCATIONAL OBJECTIVES (PEOS):

Graduates shall apply the fundamental, advanced and contemporary knowledge of

1. Electronics, Communication and allied Engineering, to develop efficient solutions and systems, to meet the needs of the industries and society.
2. Graduates will get employed or pursue higher studies or research.
3. Graduates will have team spirit, good communication skills and ethics with lifelong learning attitude.

PROGRAM OUTCOMES:

Engineering Graduates will be able to:

1. **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

RULES AND REGULATIONS OF LAB

All students must observe the Dress Code while in the laboratory.

- All bags must be placed at rack.
- The lab timetable must be strictly followed.
- Be PUNCTUAL for your laboratory session.
- Program/experiment must be executed within the given time.

Workspace must be kept clean and tidy at all time.

- Handle the systems and interfacing kits with care.
- All students are liable for any damage to the accessories due to their own negligence.
- All interfacing kits connecting cables must be RETURNED if you taken from the lab supervisor.
- Students are strictly PROHIBITED from taking out any items from the laboratory.
- Students are NOT allowed to work alone in the laboratory without the Lab Supervisor
- USB Ports have been disabled if you want to use USB drive consult lab supervisor.
- Report immediately to the Lab Supervisor if any malfunction of the accessories, is there

Before leaving the lab

- **Place the chairs properly.**
- Turn off the system properly
- Turn off the monitor.
- Please check the laboratory notice board regularly for updates.

EXPERIMENT: 1

COMMON EMITTER AMPLIFIER

AIM: - To Study the common emitter amplifier and to find

1. Cut off frequencies.
2. Bandwidth.

EQUIPMENT REQUIRED:

Name	Qty
CE Amplifier Trainer kit	1
CRO	1
Function generator	1
BNC probes and Connecting wires	1

THEORY:

The common emitter configuration is widely used as a basic amplifier as It has both voltage and current amplification.

Resistors R_1 & R_2 form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and, ensure that emitter - base junction is operating in the proper region.

In order to operate transistor as an amplifier, the biasing is done in such a way that the operating point should be in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design the V_{CE} is always set to $V_{CC}/2$. This will conform that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. Output is produced without any clipping or distortion for the maximum input signal. If not so, reduce the input signal magnitude.

The Bypass Capacitor The emitter resistor R_E is required to obtain the DC quiescent stability. However the inclusion of R_E in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance.

$$X_{CE} << R_E$$

$$\frac{1}{2\pi f C_E} << R_E$$

$$C_E >> \frac{1}{2\pi f R_E}$$

The Coupling Capacitor An amplifier amplifies the given AC signal. In order to have noiseless transmission of signal (with out DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between any two stages.

$$X_{CC} << (R_i \quad hie)$$

$$\frac{1}{2\pi f C_C} << (Ri \quad hie)$$

$$C_C >> \frac{1}{2\pi f C_C (Ri \quad hie)}$$

Frequency Response Emitter bypass capacitors are used to short circuit the emitter resistor and thus increase the gain at high frequency. The coupling and bypass capacitors cause the fall of in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitors are effectively open circuits.

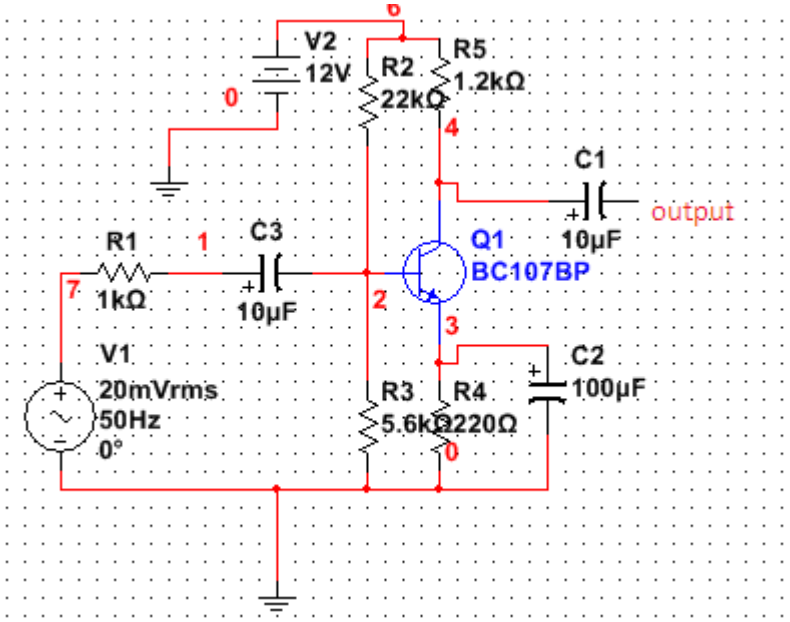
In the mid frequency range the large capacitors are effective short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence, the mid band gain is maximum.

At the high frequencies, the bypass and coupling capacitors are replaced by short circuits and stray capacitors and the transistor determine the response.

Characteristics of CE amplifier:

1. Large current gain
2. Large voltage gain
3. Large power gain
4. Current and voltage phase shift of 180^0
5. Moderated output Resistance

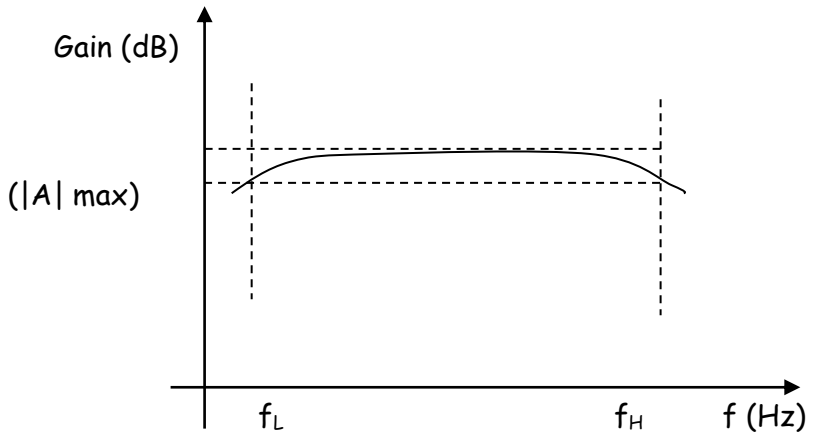
CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage V_s = 50mV (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.
4. Plot the Graph: gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.
6. Calculate all the parameters at mid band frequencies (i.e. at 1 KHz).

Graph (Frequency Response):



TABULAR COLUMN:

V_S = 50mV

Frequency	V_O (volts)	Gain = V_o/V_s	Gain (dB) =20 log (V_o/V_s)

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as f_L and f_H, and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut-off frequency and lower cut-off frequency is referred to as bandwidth ($f_H - f_L$).

RESULT

Maximum Gain=
3db Gain= Maximum Gain -3db

Band Width = $f_H - f_L$

VIVA Questions

1. How do we test the transistor for active region condition?
2. What are the factors, which influence the higher cut-off frequency?
3. What are the components, which influence the lower cut-off frequency?
4. Mention the applications of CE amplifier. Justify?
5. Compare the characteristics of CE amplifier, CB amplifier & CC amplifier.
6. What must be the voltage across the transistor, when it is operated as a switch?
7. How do we test the transistor for switching condition?

EXPERIMENT : 2

TWO STAGE RC-COUPLED AMPLIFIER

AIM To Design and study the response of a two stage RC-coupled amplifier and calculation of gain and band width.

EQUIPMENTS:

1. Function Generator, CRO : 1 No.
2. Trainer Module. : 1 No.
3. Connecting cards : 1 Lot.

THEORY:

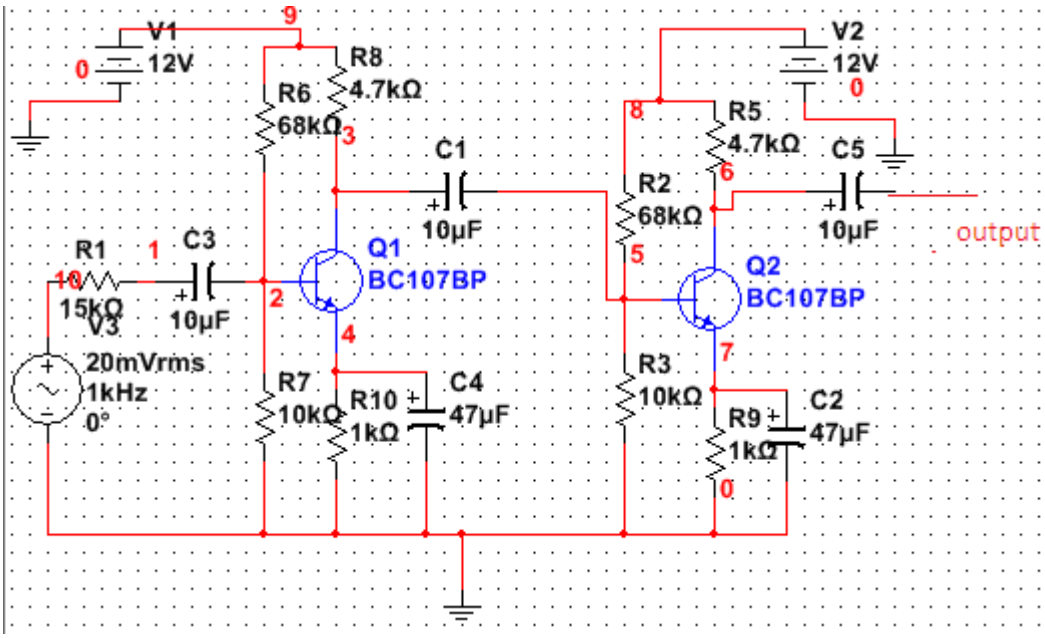
As the gain provided by a single stage amplifier is usually not sufficient to drive the load, so to achieve extra gain multi-stage amplifier are used. In multi-stage amplifiers output of one-stage is coupled to the input of the next stage. The coupling of one stage to another is done with the help of some coupling devices. If it is coupled by RC then the amplifier is called RC-coupled amplifier.

Frequency response of an amplifier is defined as the variation of gain with respective frequency. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases.

At low frequencies the reactance of coupling capacitor CC is quite high and hence very small part of signal will pass through from one stage to the next stage. At high frequencies the reactance of inter electrode capacitance is very small and behaves as a short circuit. This increases the loading effect on next stage and service to reduce the voltage gain due to these reasons the voltage gain drops at high frequencies.

At mid frequencies the effect of coupling capacitors is negligible and acts like short circuit, where as inter electrode capacitors acts like open circuit. So, the circuit becomes resistive at mid frequencies and the voltage gain remains constant during this range.

CIRCUIT:



PROCEDURE:

1. Switch on the power supply.
2. Connect the function generator with sine wave output 10 mV (peak to peak) at the input terminals.
3. And the CRO at output terminals of the first stage.
4. Measure the voltage at the first stage of amplifier.
5. Now connect the function generator to the input of the second stage and output to the CRO.

OBSERVATIONS:

V_S = _____ mV; V_{in} =_____ mV; Frequency: 10 Hz to 1 MHz

Frequency	Vo1	Vo2	Gain A_v = Vo2/ Vo1	Gain in dB	Gain

6. Measure the voltage at the second stage of the amplifier.
7. By connecting the first stage output to the second stage input measure the output voltage.
8. Now vary the input frequency from 10 Hz to 1 MHz in steps, for every value of input frequency note the output voltage and keep the input amplitude at constant value.
9. Calculate the voltage gain in decibels.
10. Plot in semi-log graph between gain Vs frequency and calculate the band width.

CALCULATIONS:

1. Determine lower cut-off frequency and upper cut-off frequency from the graph.
2. Calculate Band width.

RESULT:

Lower cut-off frequency (F_L) =

Upper cut-off frequency (F_H) =

Band width (B.W) = ($F_H - F_L$) =

VIVA –VOCE QUESTIONS:

1. What are the advantages and disadvantages of multi-stage amplifiers?
2. Why gain falls at HF and LF?
3. Why the gain remains constant at MF?
4. Explain the function of emitter bypass capacitor, C_E?
5. How the band width will effect as more number of stages are cascaded?
6. Define frequency response?
7. Give the formula for effective lower cut-off frequency, when N-number of stages is cascaded?
8. Explain the effect of coupling capacitors and inter-electrode capacitances on overall gain?
9. By how many times effective upper cut-off frequency will be reduced, if three identical stages are cascaded?
10. Mention the applications of two-stage RC-coupled amplifiers

EXPERIMENT- 3

CASCODE AMPLIFIER

AIM:

To design CASCODE amplifier with potential divider circuit using NPN Transistor 2N2923 for the specifications: I_C= 3 mA, Vce = 10v,β = 190, & $I_{R1} = 32I_B$ .verify DC values (Voltage and current) at various nodes.

APPARATUS: -

1. Trainer Kit
2. Function generator
3. Power Supply
4. CRO

DESIGN PROCEDURE:

Vcc = 25V

Select $V_{RE} \leq V_{CE}$

Select V_{RE} = 5V

$$\therefore R_E = \frac{V_{RE}}{I_C} = \frac{5}{3m} = 1.66K(select 2.00K)$$

& $V_{RC}=V_{CC}-V_{CE}-V_{RE}=25-10-5=10V$

$$\therefore R_C = \frac{V_{RC}}{I_C} = \frac{10}{3m} = 3.33K\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{3m}{190} = 15\mu A$$

$$\therefore I_{R1} = 32I_B = 32 \times 15\mu = 480\mu A$$

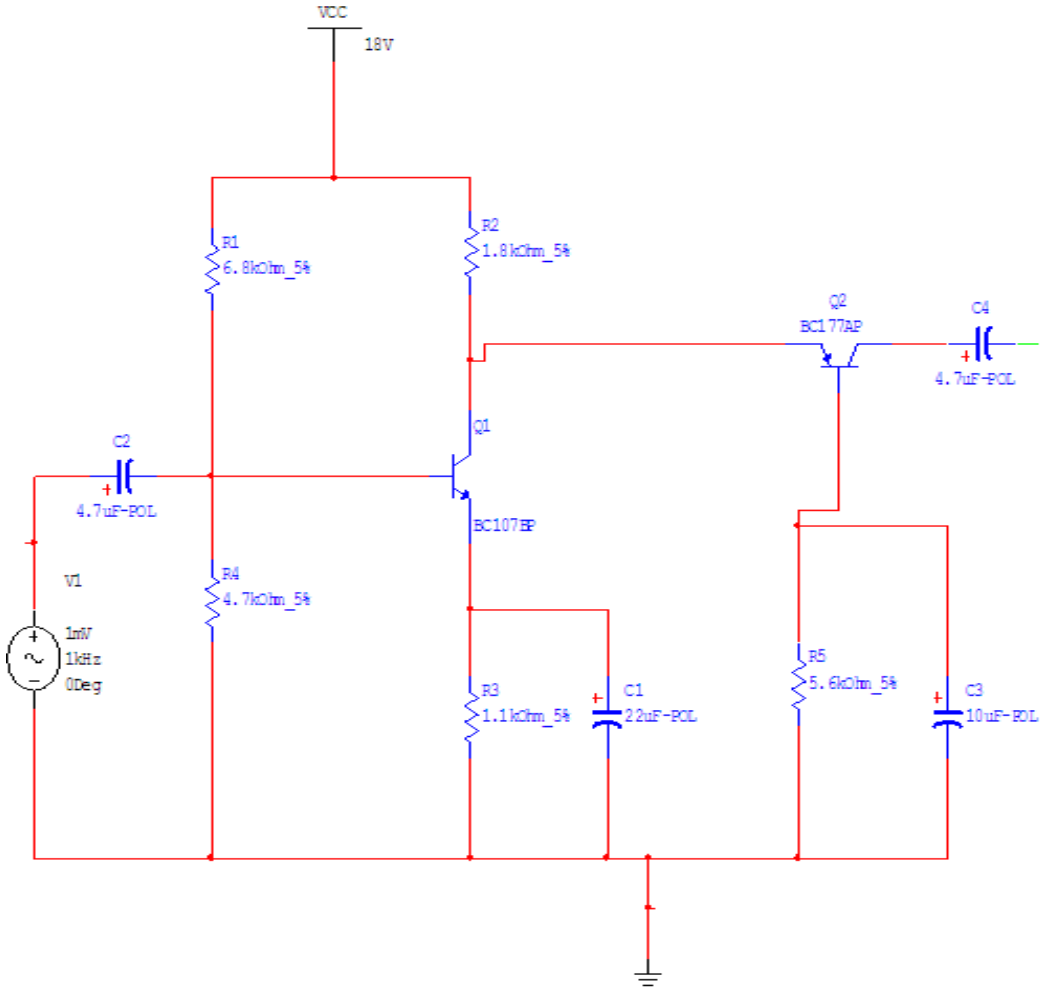
$$\therefore I_{R2} = I_{R1} - I_B = 480 - 15 = 465\mu A$$

$$\& V_B = V_{BE} + V_{RE} = 0.65 + 5 = 5.65V$$

$$\therefore R_2 = \frac{V_B}{I_{R2}} = \frac{5.65}{465\mu} = 12.15K\Omega$$

$$R_1 = \frac{V_{CC} - V_B}{I_{R1}} = \frac{25 - 5.65}{480\mu} = 40.3125K\Omega$$

CIRCUIT DIAGRAM:



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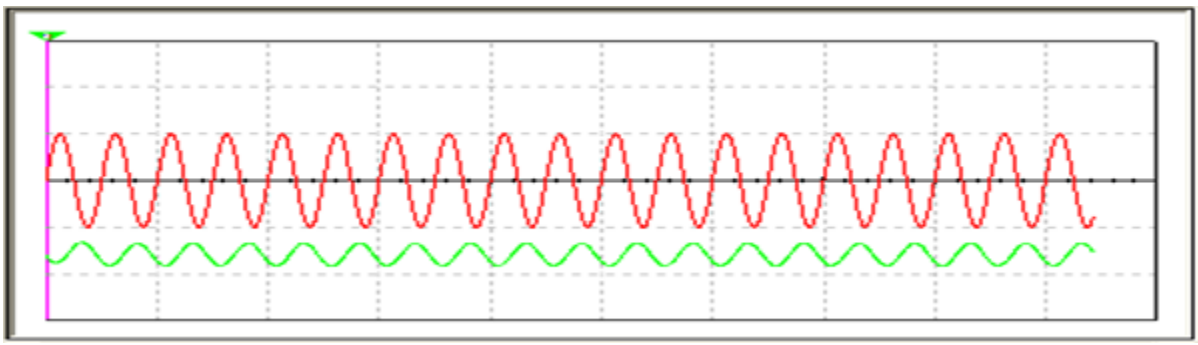
PROCEDURE:

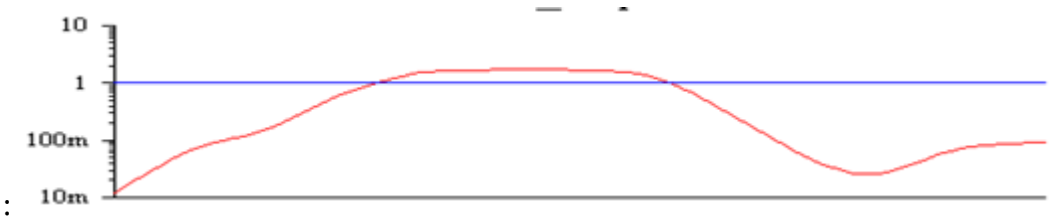
1. Connect the circuit as per the Diagram

2. For a fixed value of input voltage vary the frequency of input signal and note down the corresponding output voltage and draw the Transfer characteristics

EXPECTED WAVEFORM:



FREQUECNY RESPONSE



:

RESULT:

EXPERIMENT- 5
CURRENT SHUNT FEEDBACK AMPLIFIER

AIM: To study and Design current shunt feedback amplifier with a feedback resistance 4.7 KΩ using transistor BC 107.

APPARATUS

1. **Trainer Kit** **1**
2. **CRO** **1**
3. **Function Generator** **1**
4. **Connecting Wires**.

DESIGN PROCEDURE:

$$\beta = \frac{-I_F}{I_E} = \frac{R_E}{R_F + R_E} = \frac{470}{5K + 470} = 0.085$$

$$A_I = \frac{I_R}{I_S} = \frac{-I_{C2}}{I_{B2}} \times \frac{I_{B2}}{I_{C1}} \times \frac{I_{C1}}{I_{B1}} \times \frac{I_{B1}}{I_S}$$

$$\frac{I_{C2}}{I_{B2}} = -hFE = -50, \frac{I_{C1}}{I_{B1}} = hFE = 50$$

$$\frac{I_{C2}}{I_{C1}} = \frac{-R_{C1}}{R_{C1} + R_{I2}} = \frac{2.2K}{2.2K + 1.076K} = 0.67151$$

$$\frac{I_{B1}}{I_S} = \frac{R}{R + hie} = \frac{4K}{4K + 1.1K} = 0.8; Where\ R = R_S\ //(470 + 5K) = 4K$$

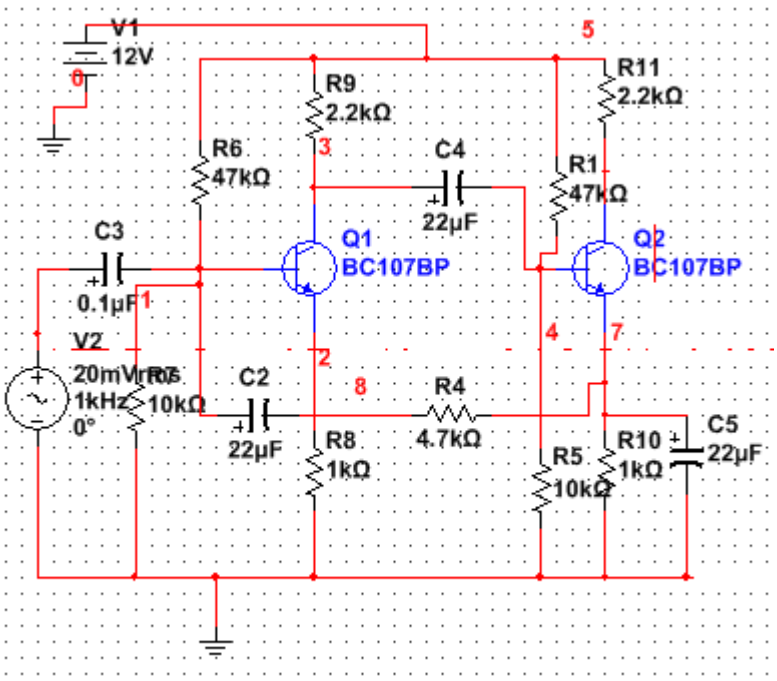
$$A_I = -(-50)(0.67151)(50)(0.8) = 1.343K$$

$$D = 1 + \beta A_I = 1 + (0.085)(1.343K) = 115.15$$

$$A_{IF} = \frac{A_I}{D} = \frac{1.343K}{115.15} = 11.66$$

$$\therefore A_{VF} = \frac{V_0}{V_S} = \frac{I_O\ R_{C2}}{I_S\ R_S} = A_{IF}\ \frac{R_{C2}}{R_S} = 11.66 \times \frac{2.2K}{15K} = 1.71$$

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are made as per circuit diagram.

2. Keep the input voltage constant at 20mV peak-peak and 1kHz frequency note down the output voltage and calculate the gain by using the expression

$$A_v = 20\log(V_0 / V_i)\ dB$$

3. Connect the Emitter Feedback Resistor and repeat STEP 2.And observe the effect of feedback on the gain of the amplifier.
4. For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.
5. Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression $A_v = 20\log (V_0 / V_i)\ dB$
6. A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph

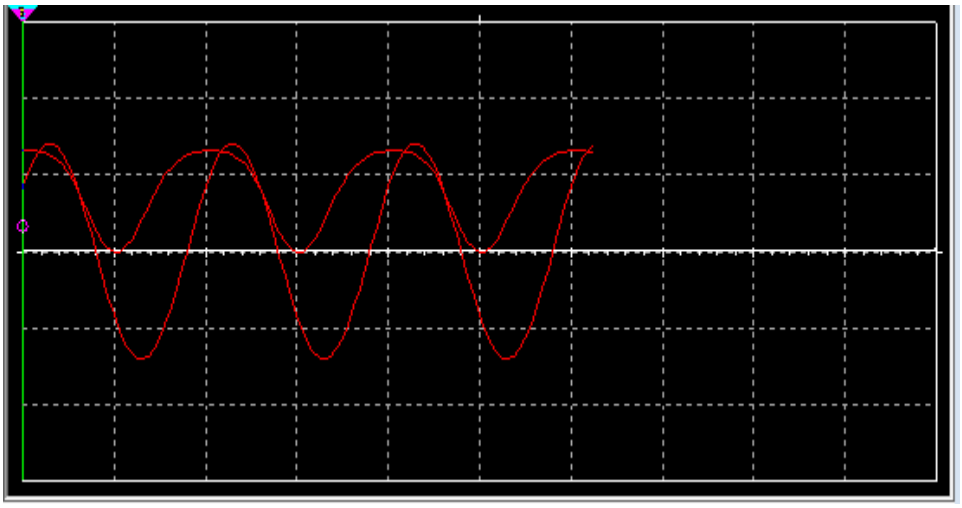
7. The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = $f_2 – f_1$.

Where f_1 is lower cutt off frequency of CE amplifier f_2 is upper cutt off frequency of CE amplifier

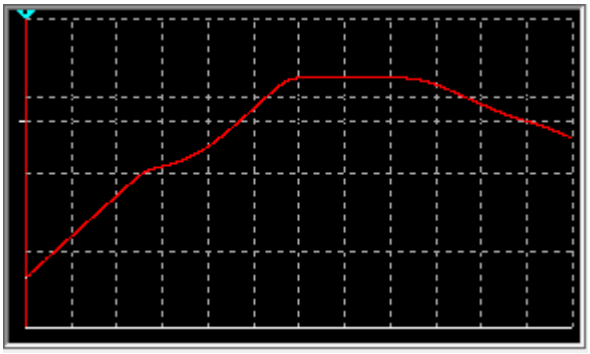
The gain-bandwidth product of the amplifier is calculated by using the expression

Gain-Bandwidth Product = 3-dB midband gain X Bandwidth.

EXPECTED WAVEFORMS



FREQUENCY RESPONSE:



Tabular Columns:

S.NO	Output Voltage (V_o) with feedback	Output Voltage (V_o) without feedback	Gain(dB) with feedback	Gain(dB) without feedback

Voltage Gain: V_i = 20 mV

RESULT:

The current shunt feed back amplifier is designed with feed back resistance of 4.7KΩ The Output waveform and frequency response are observed.

CONCLUSION:-

VIVA QUESTIONS:

1. What is feedback in Amplifiers?
2. Explain the terms feed back factor and open loop gain.
3. What are the types of feedback?
4. Explain the term negative feedback in amplifiers?
5. What are the disadvantages of negative feedback?
6. What are the advantages of negative feedback?
7. When will a negative feedback amplifier circuit be unstable?
8. Compare the negative feedback and Positive feedback.
9. Give the expression for closed loop gain for a negative feed back amplifier?
10. How does negative feedback reduce distortion in an amplifier?
11. How does series feedback differ form shunt feedback?
12. What is the difference between voltage feedback and current feedback?

Experiment : 6

VOLTAGE SERIES FEEDBACK AMPLIFIER

Aim:

To plot the frequency response characteristics of voltage series feedback amplifier.

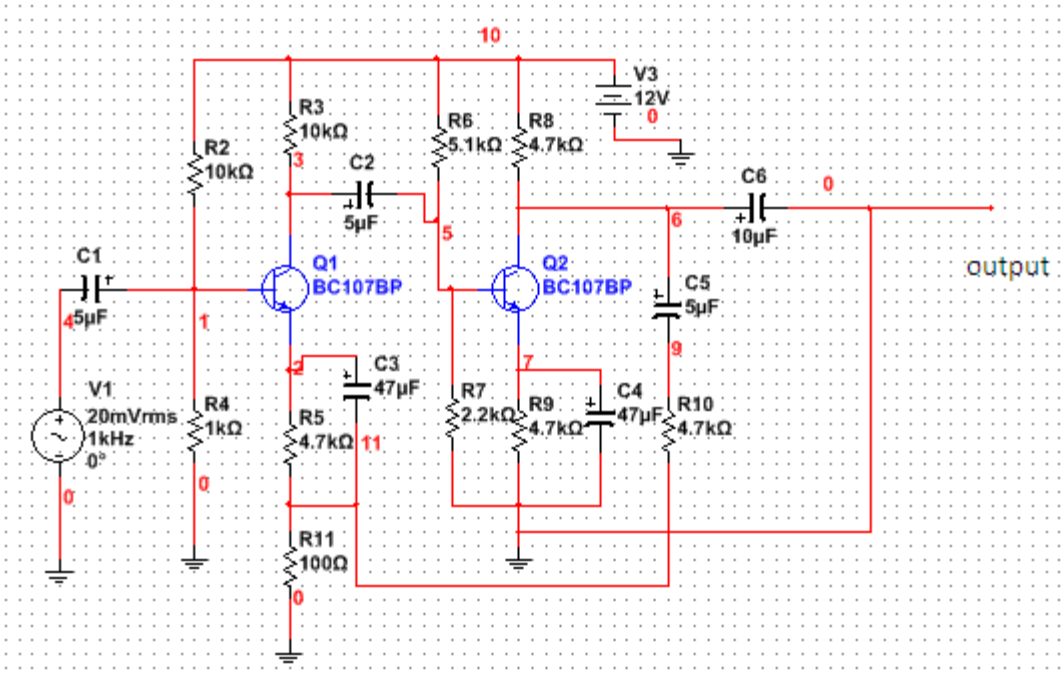
Apparatus Required:

TRAINER KIT

Function generator,

CRO

Circuit Diagram:



THEORY:

When any increase in the output signal results into the input in such a way as to cause the decrease in the output signal, the amplifier is said to have negative feedback.

The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by proper use of this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased.

In Current-Series Feedback, the input impedance and the output impedance are increased. Noise and distortions are reduced considerably.

PROCEDURE:

1. Connections are made as per circuit diagram.

2. Keep the input voltage constant at 20mV peak-peak and 1 kHz frequency. For different values of load resistance, note down the output voltage and calculate the gain by using the expression

$$A_v = 20\log (V_0 / V_I) \text{ dB}$$

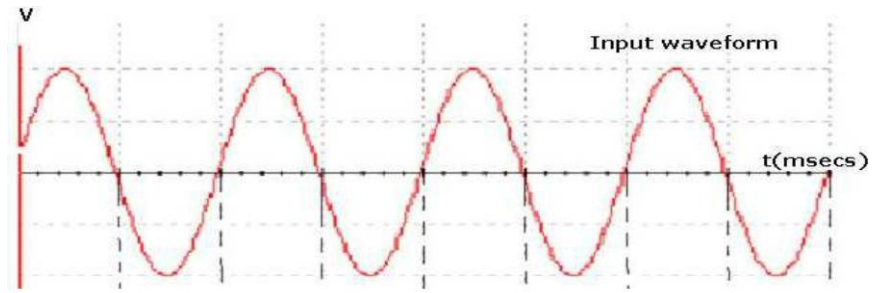
8. Remove the emitter bypass capacitor and repeat STEP 2.And observe the effect of feedback on the gain of the amplifier.
9. For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.
10. Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression $A_v = 20\log (V_0 / V_i)$ dB
11. A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph

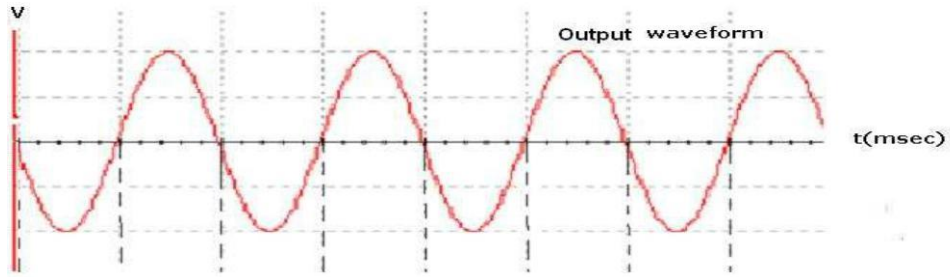
12. The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = $f_2 - f_1$.

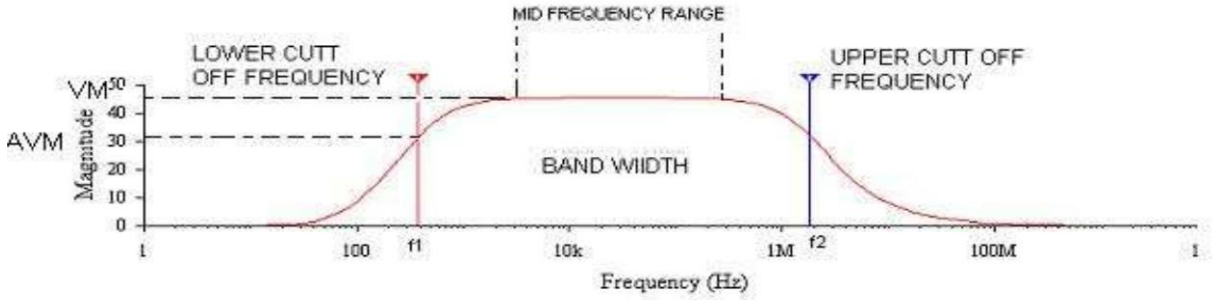
Where f_1 is lower cutt off frequency of CE amplifier f_2 is upper cutt off frequency of CE amplifier

The gain-bandwidth product of the amplifier is calculated by using the expression Gain-Bandwidth Product = 3-dB midband gain X Bandwidth.

EXPECTED WAVEFORM:







Tabular Columns:

S.NO	Output Voltage (V_o) with feedback	Output Voltage (V_o) without feedback	Gain(dB) with feedback	Gain(dB) without feedback

PRECAUTIONS:

1. While taking the observations for the frequency response, the input voltage must be maintained constant at 20mV.
2. The frequency should be slowly increased in steps.
3. The three terminals of the transistor should be carefully identified.
4. All the connections should be correct.

RESULT:

EXPERIMENT- 7

RC PHASE SHIFT OSCILLATOR USING TRANSISTORS

AIM:

a) Design RC phaseshift oscillator to have resonant frequency of 6KHz.
Assume R_1 = 100k, R_2 = 22K, R_C = 4 K ,R_E =1K & V_{CC} = 12V.

b) Obtain h_{fe} for the above designed value for $A_V > -29$, $R \geq 2 R_C$.

APPARATUS: NI Multisim 14.0 Software, PC.

DESIGN PROCEDURE:

a) Let R = 10K

$$f_r = \frac{1}{2\pi R_C \sqrt{6+4K}} \quad When \quad K = \frac{R_C}{R}$$

$$\therefore C = \frac{1}{2\pi \times 10K \times 6K \sqrt{6+4\times\frac{4K}{10K}}}$$

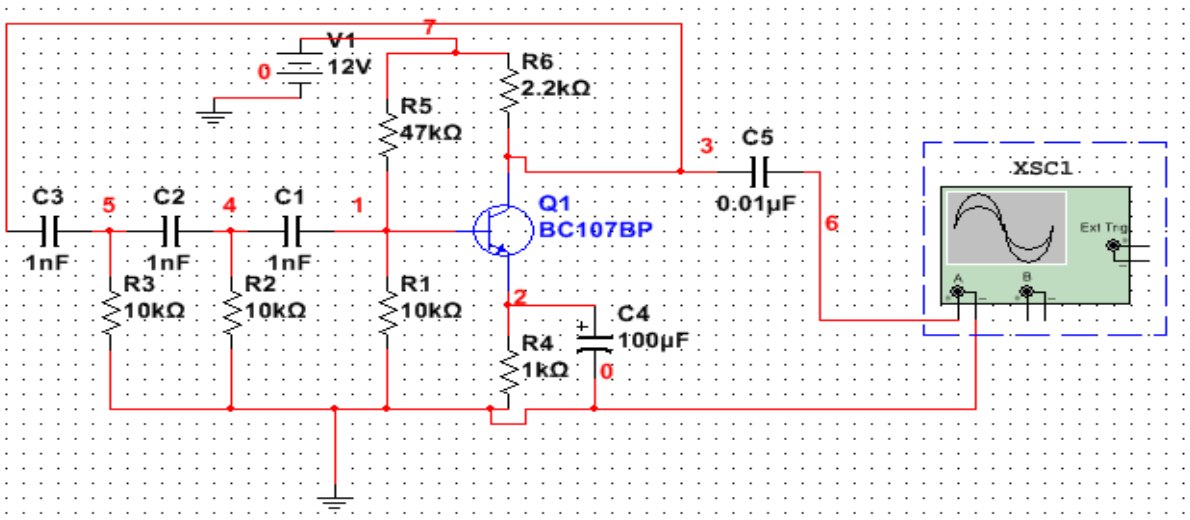
$$= 0.962nF \approx 1nF \quad (Select\ s\tan dard)$$

$$\therefore R = 10K \ ; \quad C = 1nF$$

$$b) \quad hfe \geq 23 = \frac{29}{K} + 4K \quad for\ \ sustained\ \ oscillation$$

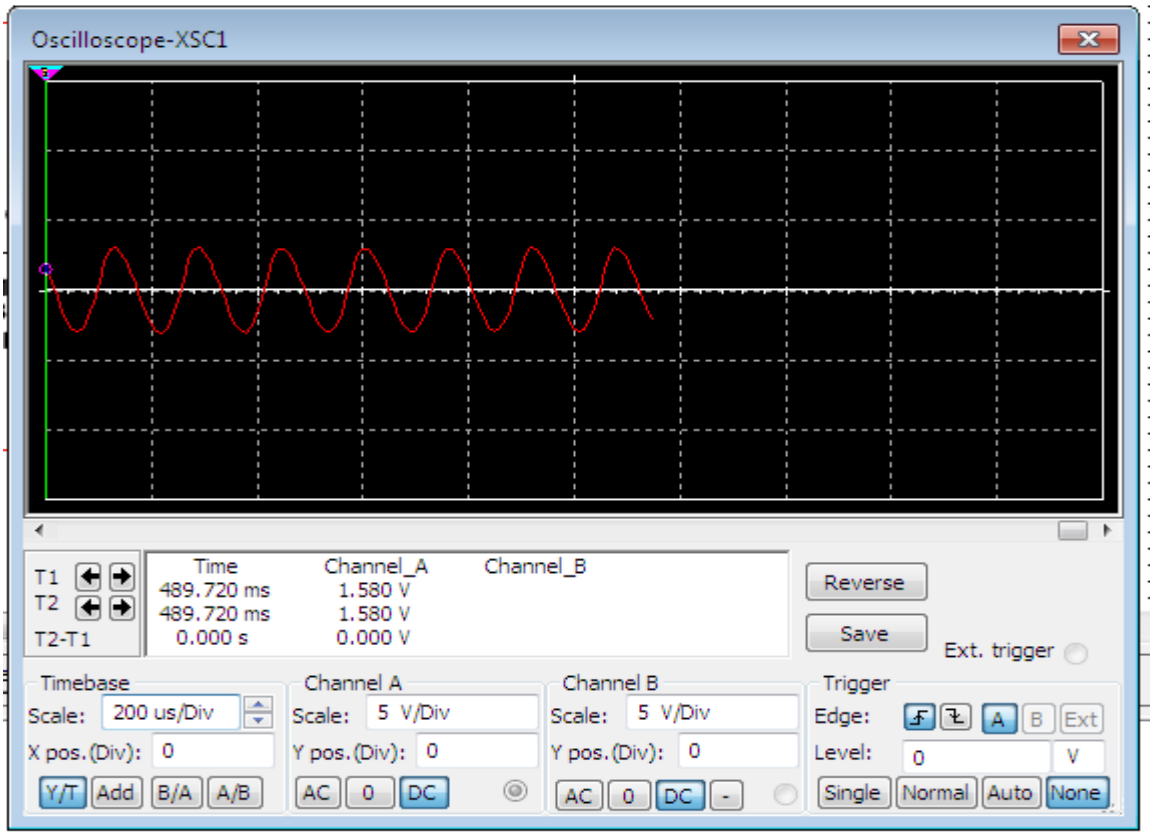
$$= 97.1$$

CIRCUIT DIAGRAM:



PROCEDURE:

Design the circuit using multisim software and verify the results using Oscilloscope.



RESULT:- RC phase shift oscillator with f_r =6KHz is designed. The value of h_{fe} for the designed value is computed.

CONCLUSION:-

VIVA QUESTIONS:

1. What is an Oscillator circuit?

2. What is the main difference between an amplifier and an oscillator?

3 State Barkhausen criterion for oscillation.

4. State the factors on which oscillators can be classified.

5. Give the expression for the frequency of oscillation and the minimum gain required for sustained oscillations of the RC phase shift oscillator.

6. Why three RC networks are needed for a phase shift oscillator? Can it be two or four?

7. What are the merits and demerits of phase shift oscillator?

8 At low frequency which oscillators are found to be more suitable?

9 What are the two important RC oscillators?

10 What makes Quartz produce stable oscillations?

11. What are the factors which contribute to change in frequency in oscillators?

EXPERIMENT 8

HARTLEY OSCILLATOR

AIM: To study the Hartley oscillator and to find the frequency of the oscillations.

EQUIPMENT REQUIRED:

NI Multisim 14.0 Software, PC**.**

THEORY:

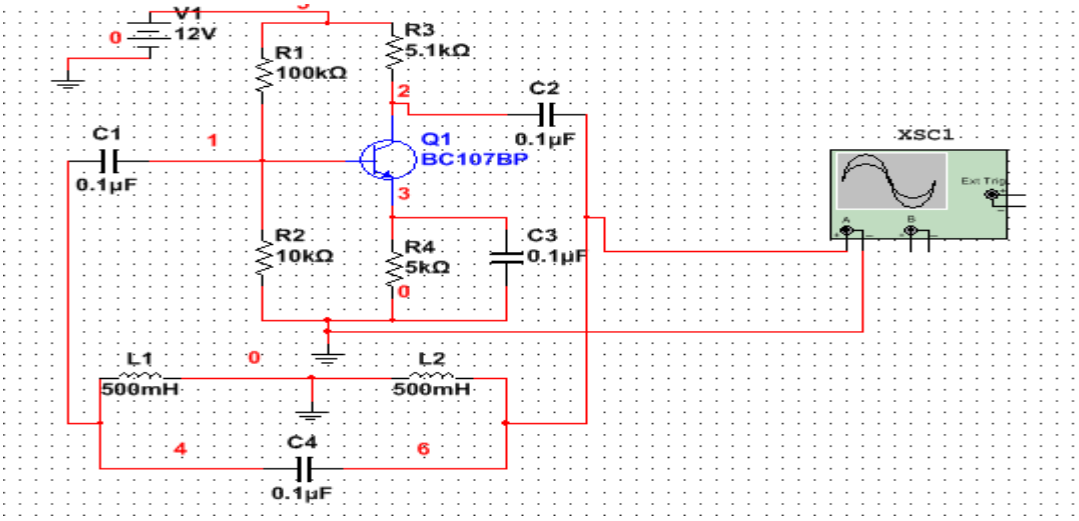
Hartley oscillator is a variable frequency RF oscillator. It is commonly used as a local oscillator in radio receivers. It has two main advantages: adaptability to a wide range of frequencies and is easy to tune. It works on the principle of parallel resonance. The total inductance of the tank circuit is divided into two parts L1 & L2 connected in series and the combination works as a autotransformer. The capacitor blocks the d.c. component. The resistor R provides the necessary base-emitter bias. Hartley is also called tapped inductance Oscillator.

The frequency of oscillations is given by:

$f_o = 1/2\pi\sqrt{(L_T C)}$ Where $L_T = L1 + L2$

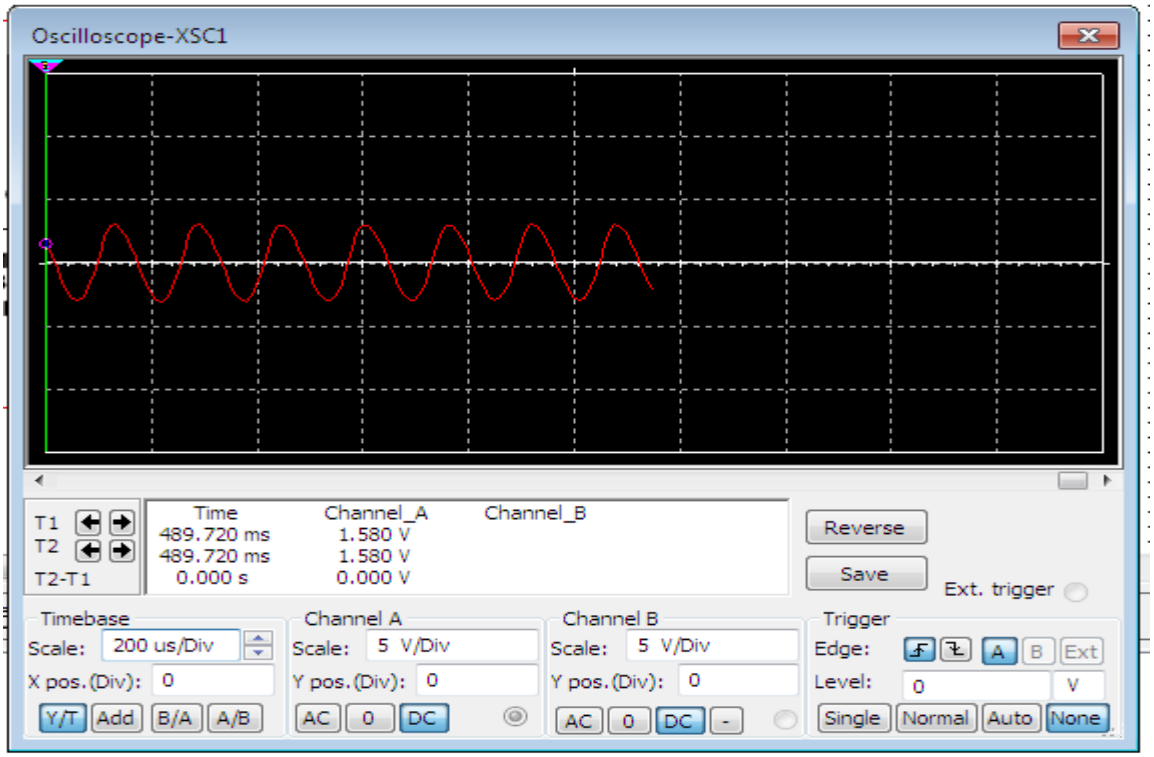
Variation of the variable inductor can alter the frequency of oscillations.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Instruments ---- Oscilloscope



RESULTS:-

The common base high frequency amplifier is designed. Also DC voltages currents are observed. The Bandwidth is far greater than the bandwidth of the CE amplifier

x

CONCLUSION:

VIVA QUESTIONS:

1. What type of feedback is preferred in oscillators?
2. How does oscillation start in oscillators?
3. List out the applications of oscillators
4. Which oscillator is very suitable for audio range applications?
5. Which oscillator is suitable for RF range applications?
6. Which oscillator is suitable for low frequency applications? t
7. Amplifier circuit is necessary in an oscillator, why?
8. Three RC sections are used in RC Phase Shift oscillators why?
9. Generally negative feedback is employed in amplifiers whereas positive feedback is employed in oscillators, why?
10. For low frequency applications, we apply RC oscillators and not LC oscillators why

EXPERIMENT 9

COLPITTS OSCILLATOR

AIM: To study the Colpitts oscillator and to find the frequency of the oscillations.

x

APPARATUS REQUIRED:

NI Multisim 14.0 Software, PC.

THEORY:

Colpitt's oscillator is a sine-wave feedback oscillator of L-C type. It is a variable frequency RF oscillator. It works on the principle of parallel resonance. The total capacitance of the tank circuit is divided into two parts C1 & C2 connected in series. Colpitt's oscillator is also called tapped capacitance Oscillator.

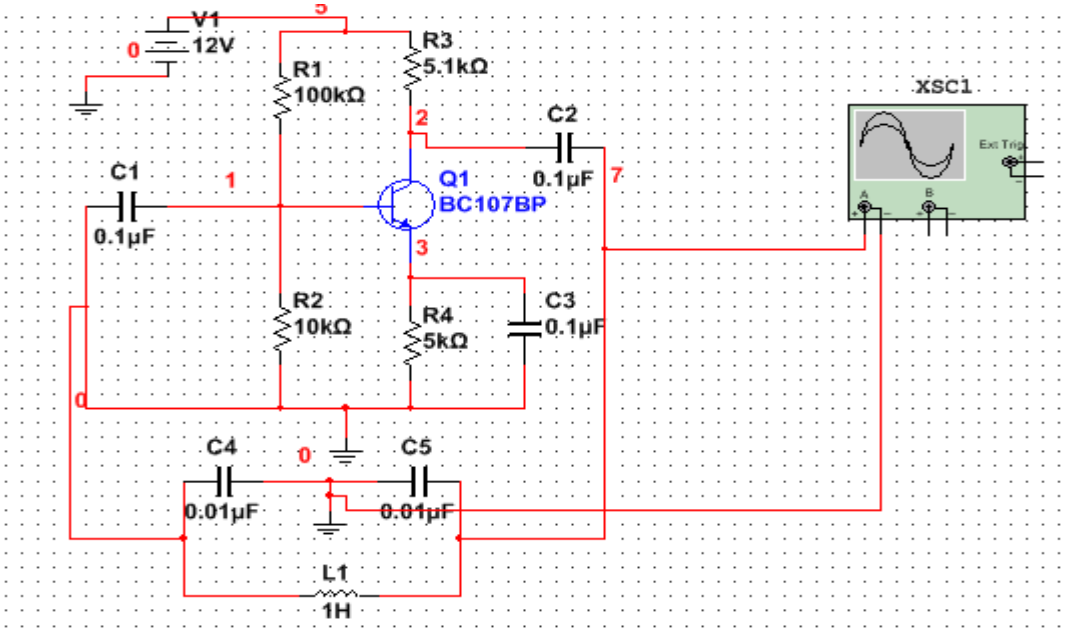
The frequency of oscillations is given by:

$f_o = 1/[2\Pi \sqrt{(LC_T)}]$ Where $C_T = C_1C_2/ (C_1 + C_2)$

The condition for sustained oscillations in the circuit is

$h_{fe} >= C_1/C_2$

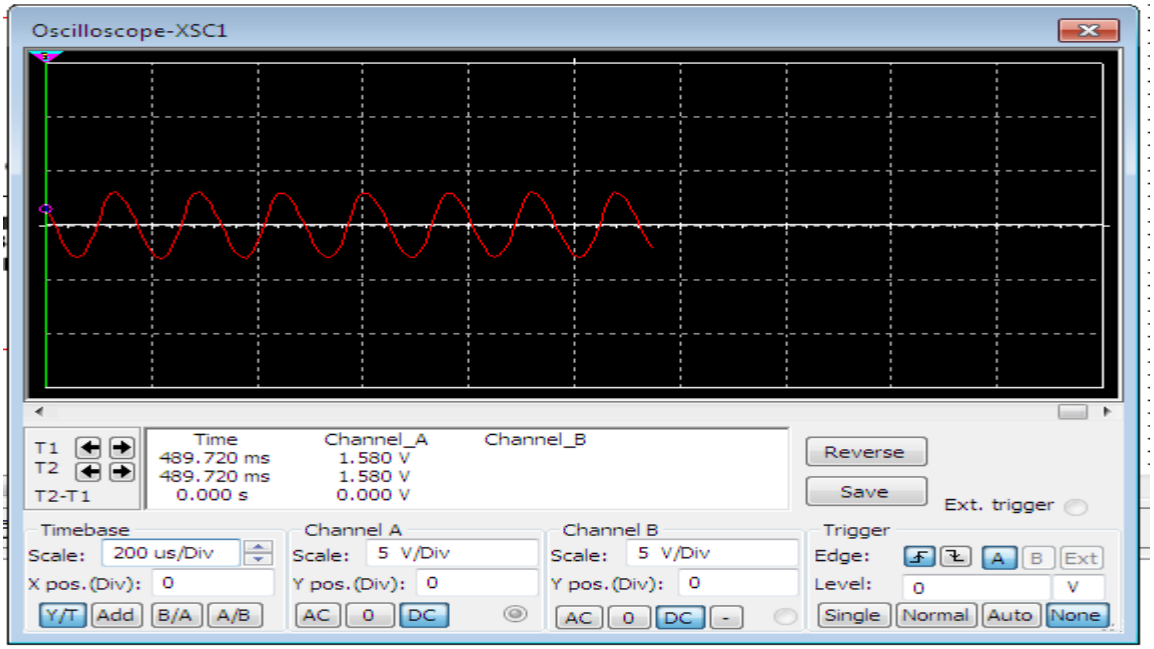
CIRCUIT DIAGRAM:



Varying the variable inductor can alter the frequency of oscillations.

PROCEDURE:

1. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Instruments ---- Oscilloscope



RESULTS:-

The common base high frequency amplifier is designed. Also DC voltages currents are observed. The Bandwidth is far greater than the bandwidth of the CE amplifier

CONCLUSION:-

VIVA QUESTIONS:

1. What type of feedback is preferred in oscillators?
2. How does oscillation start in oscillators?

3. List out the applications of oscillators
4. Which oscillator is very suitable for audio range applications?
5. Which oscillator is suitable for RF range applications?
6. Which oscillator is suitable for low frequency applications?
7. Amplifier circuit is necessary in an oscillator, why?
8. Three RC sections are used in RC Phase Shift oscillators why?
9. Generally negative feedback is employed in amplifiers whereas positive feedback is employed in oscillators, why?
10. For low frequency applications, we apply RC oscillators and not LC oscillators why

EXPERIMENT- 10

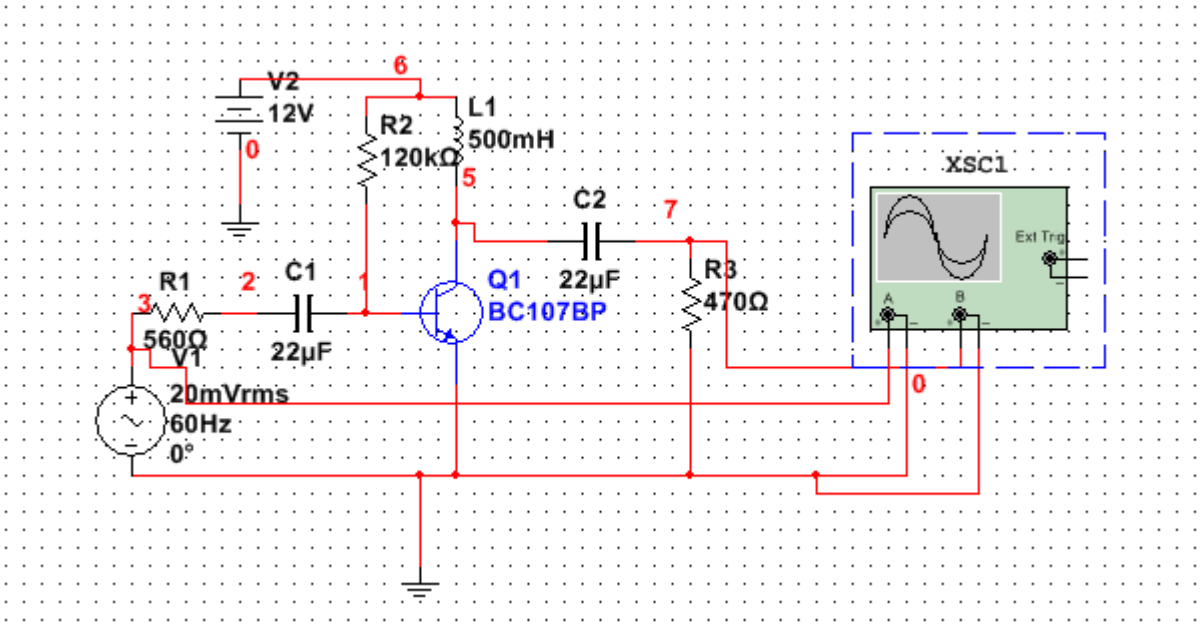
CLASS A Power Amplifier(TRANSFORMERL ESS)

AIM :

To study the operation of Class A power amplifiers.

APPARATUS: NI Multisim 14.0 Software, PC.

CIRCUIT DIAGRAM:



THEORY:

The classification of amplifiers is based on the position of the quiescent point and extent of the characteristics that is being used to determine the method of operation.

There are 4 classes of operations. They are

1. Class A 2.Class AB 3.Class B 4.Class C

CLASS A: - In class A operation the quiescent point and the input signal are such that the current in the output circuit (at the collector) flows for all times. Class A amplifier operates essentially over a linear portion of its characteristic there by giving rise to minimum of distortion.

CLASS B: - In class B operation, the quiescent point is at an extreme end of the characteristic, so that under quiescent conditions the power drawn from the dc power supply is very small .If the input signal is sinusoidal, amplification takes place for only half cycle.

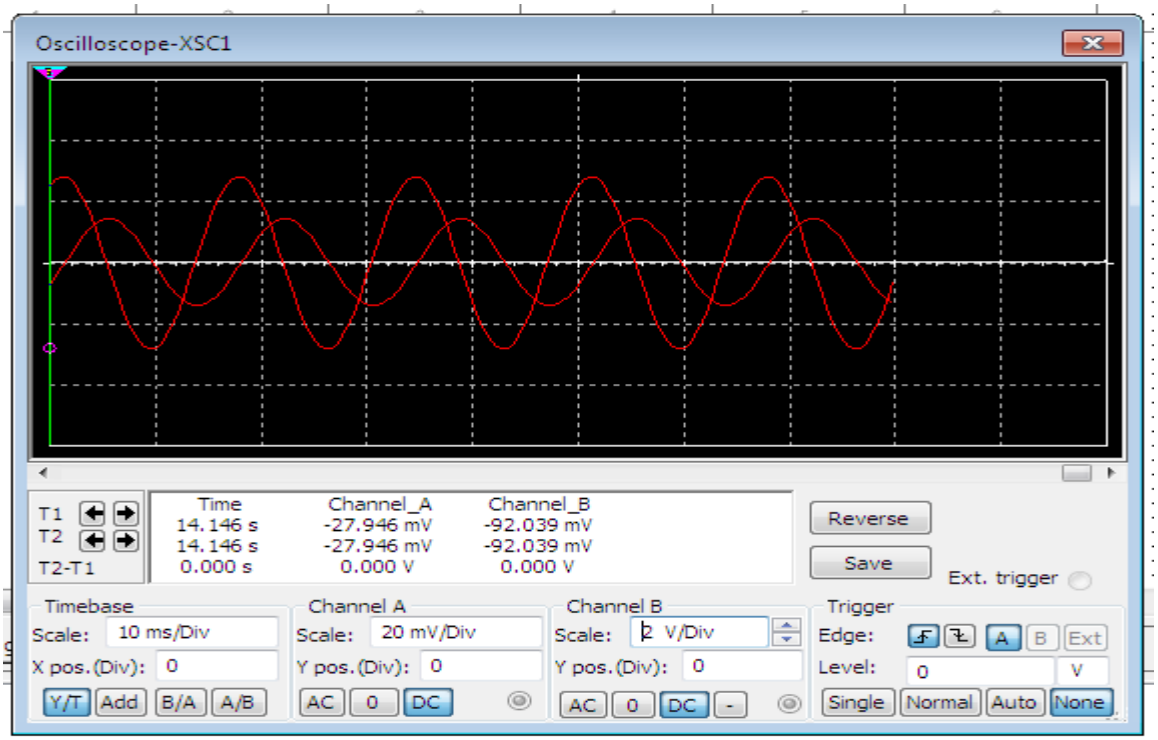
CLASS AB: - A class AB amplifier is the one that operates between the two extremes defined for class A and Class B. Hence the output signal exists for more than 180^0 of the input signal.

CLASS C: - In class C operation, the quiescent operating point is chosen such that output signal (voltage or current) is zero for more than on half of the input sinusoidal signal cycle.

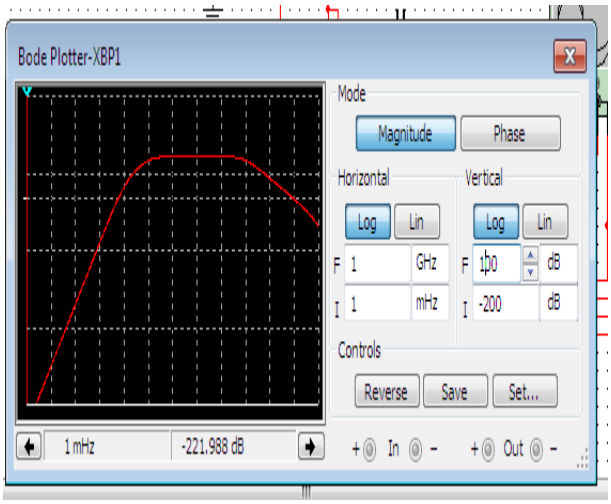
PROCEDURE:

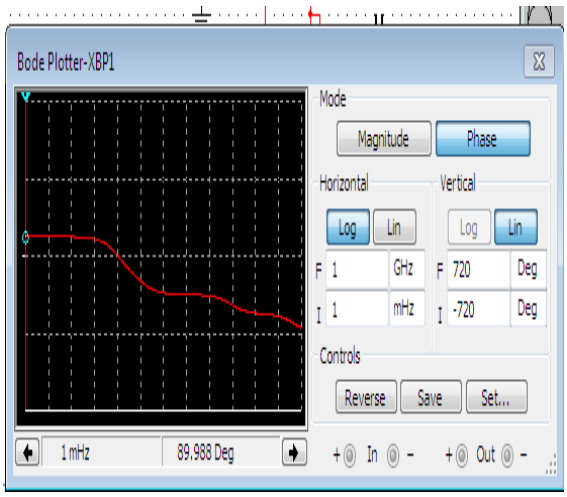
1. An input sine wave (peak-peak) of 20mV is applied to the circuit.
2. Connect the output to the C.R.O.
3. Varying R_3 value, observe and record the output waveforms for different classes of operation.
4. Also observe the V_i & V_o waveforms using parameter sweep for different classes of operation.

1. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Instruments ---- Oscilloscope).



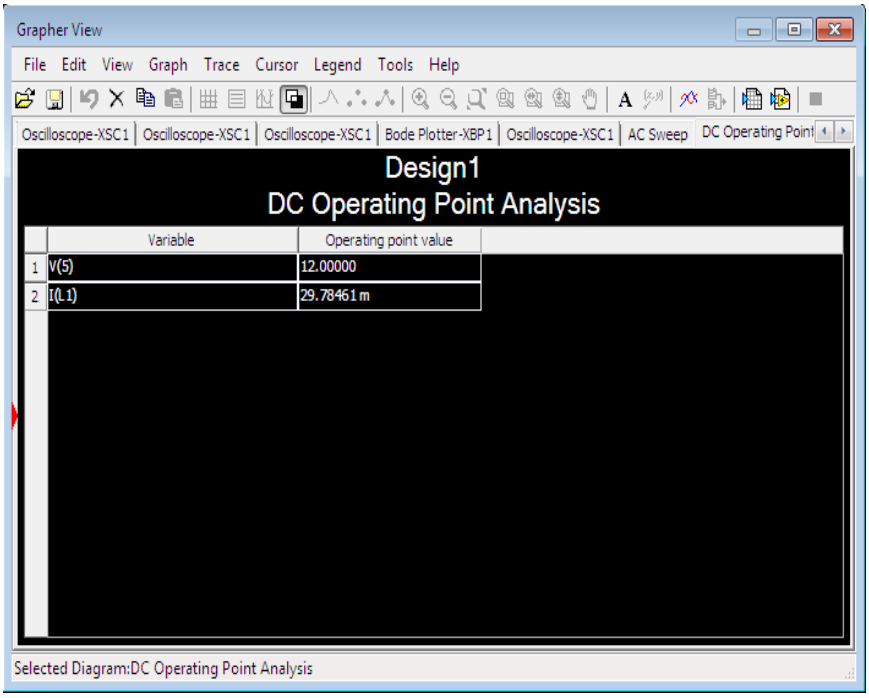
2. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Instruments ---- Bode Plotter).



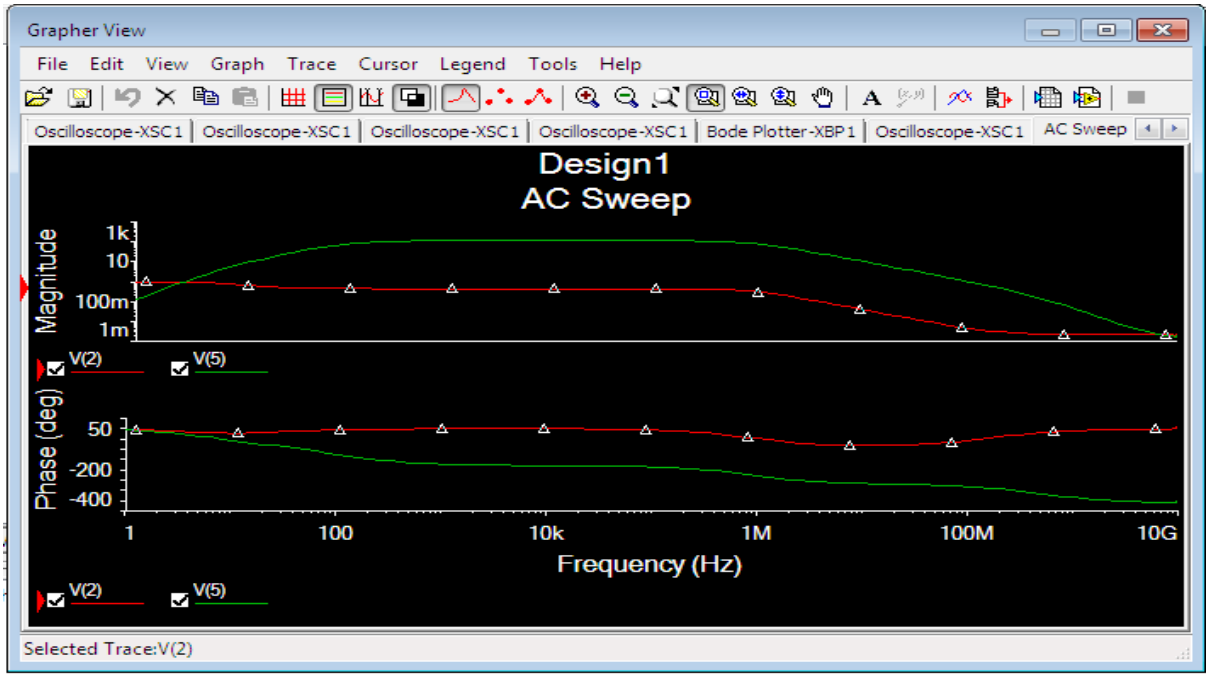


3. Design

the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Analysis ---- DC Operating point



6. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ----- Analysis ---- AC Analysis).



RESULT:

1. In class A amplifier output current flows for whole 360^0
2. In class AB power amplifier output current flows between 180^0 and 360^0
3. In class B power amplifier output current flows for 180^0
4. In Class C power amplifier output current flows for less than 180

CONCLUSION:-

VIVA QUESTIONS:

1. How do you bias class A operation?
2. What is conversion efficiency?
3. Define Class A mode of operation.
4. What are the advantages & disadvantages of Class A mode of operation?
5. Distinguish between voltage and power amplifier?
6. Which power amplifier gives minimum distortion?
7. What are the drawbacks of class A amplifier?
8. In Which class of amplifier, the efficiency is high? And why?
9. Classify power amplifiers on the basis of the mode of operation.
10. Give two drawbacks of Class A power amplifier.

EXPERIMENT- 11

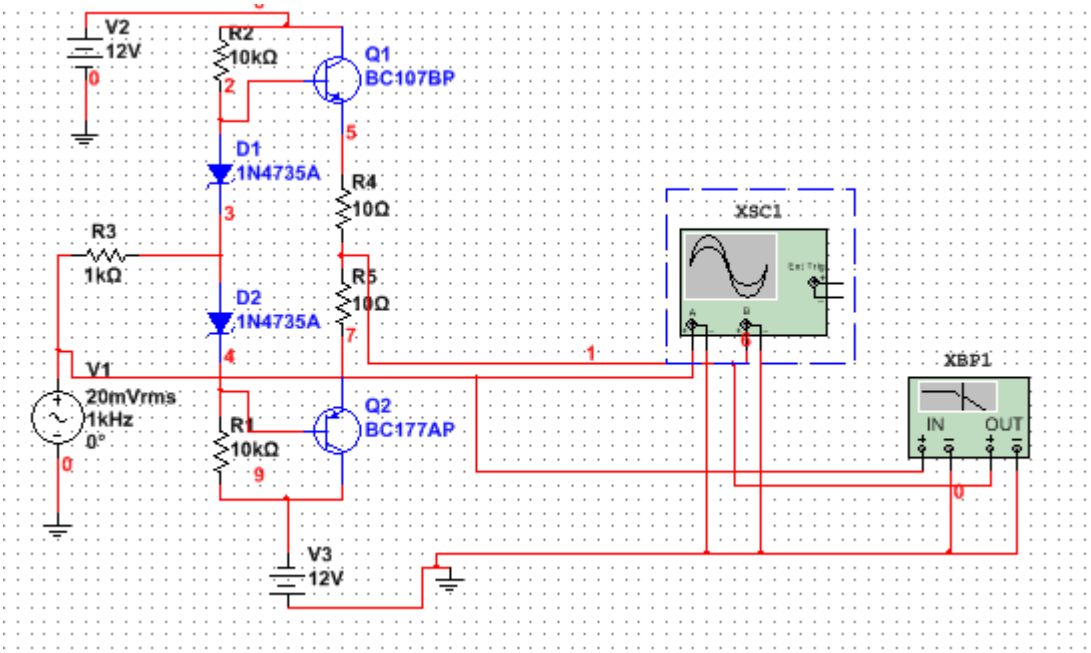
CLASS B COMPLEMENTARY SYMMETRY AMPLIFIER

AIM :

To study the operation of Class B complementary symmetry amplifiers.

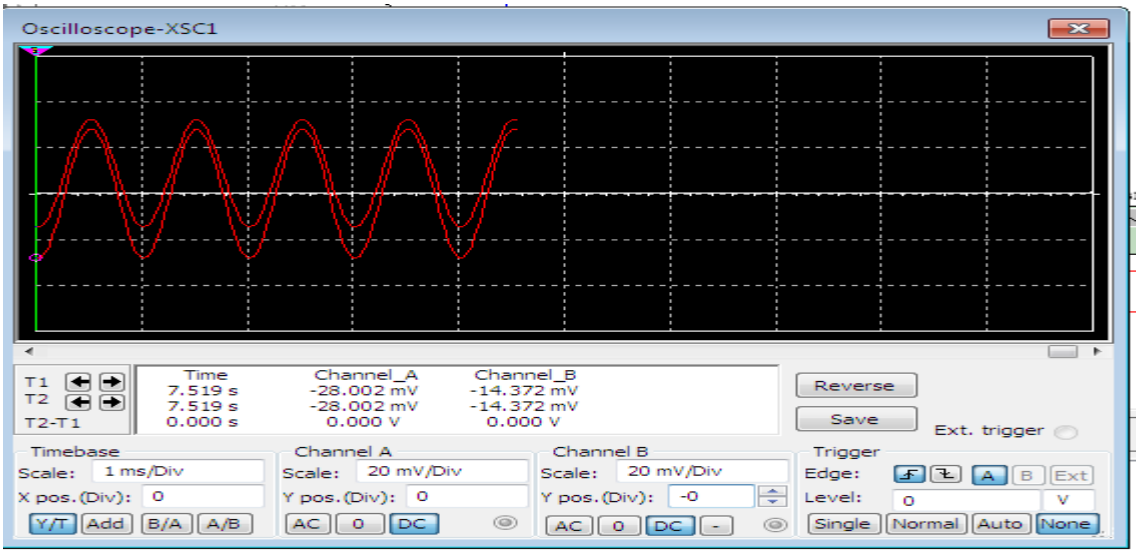
APPARATUS: Multisim software, PC.

CIRCUIT DIAGRAM:

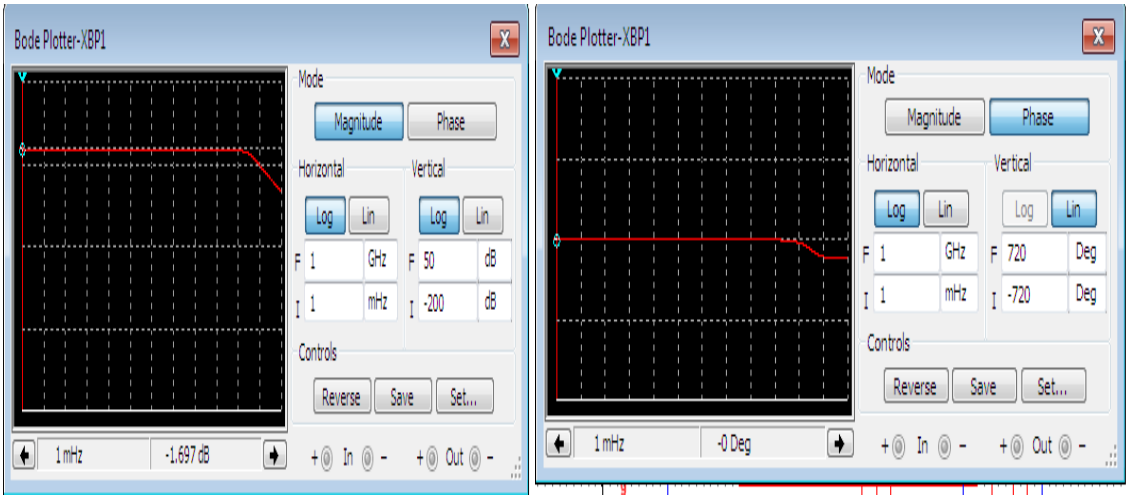


PROCEDURE:

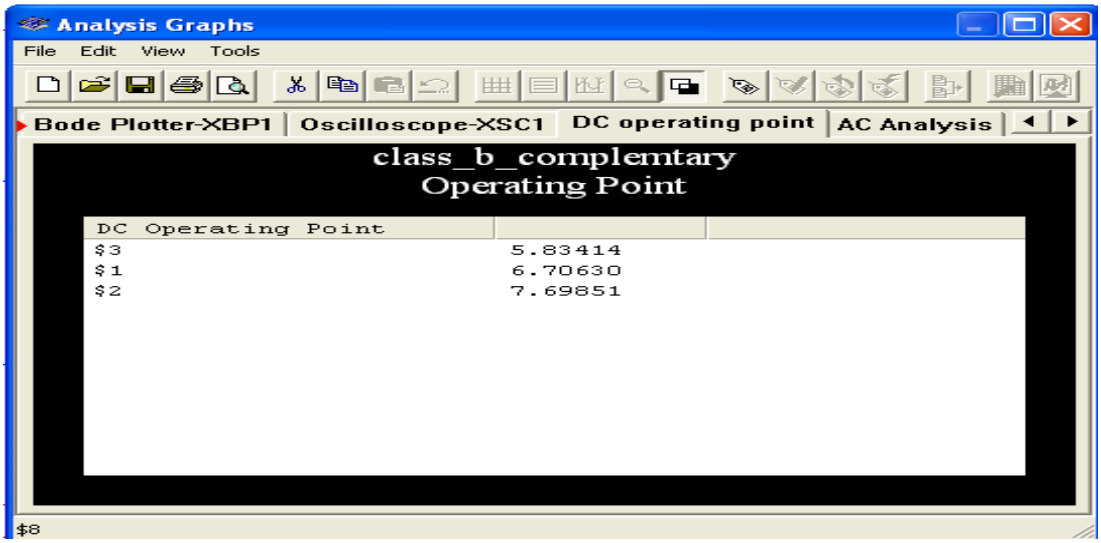
1. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Instruments ---- Oscilloscope).



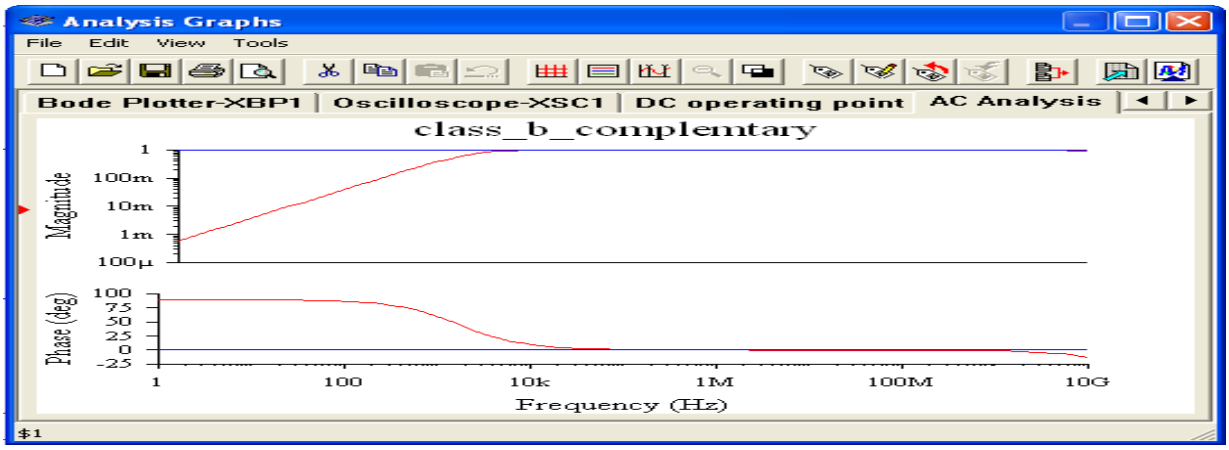
2. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Instruments ---- Bode Plotter).



3. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Analysis ---- DC Operating point).



4. Design the circuit using multisim software and verify the results using oscilloscope (Simulate ---- Analysis ---- AC Analysis).



RESULT:

The Class B Complementary Symmetry Amplifier is designed. The D.C operating point and AC Analysis taken at various nodes are observed.

CONCLUSION:-

VIVA QUESTIONS:

1. How do you bias class B operation?
2. What is conversion efficiency?
3. Define Class B mode of operation.
4. What are the advantages & disadvantages of Class B mode of operation?
5. Distinguish between voltage and power amplifier?
6. Which power amplifier gives minimum distortion?
7. What are the drawbacks of class C amplifier?
8. In Which class of amplifier, the efficiency is high? And why?
9. Classify power amplifiers on the basis of the mode of operation.
10. Give two drawbacks of Class B power amplifier.

ADD ON EXPERIMENTS

UJT RELAXATION OSCILLATOR

AIM : *To obtain a saw tooth waveform using UJT and test its performance as an oscillator*

APPARATUS :

1. Resistors 47k , 100
2. Capacitor - 0.1 F
3. 2n2646 UJT
4. Bread board
5. Power supply (0-30V)
6. CRO(1Hz-20MHz)

THOERY :

'*A Unijunction transistor (UJT), as the very implies, has only one p-n junction, unlike a BJT which has two p-n junctions'.*

The equivalent circuit of the U JT is as shown in figure1.

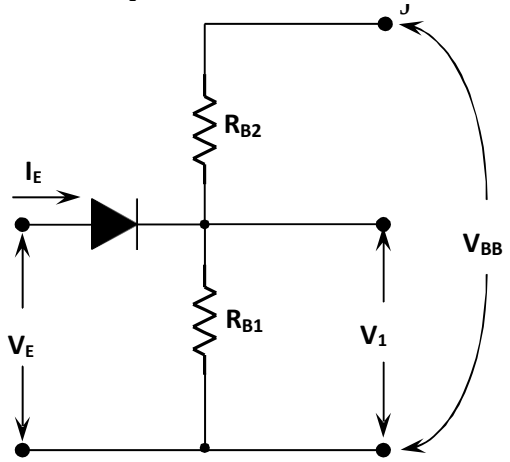


Figure:1

R_{B1} is the resistance between base B_1 and the emitter, and it is basically a variable resistance, its value being dependent upon the emitter current I_E.

R_{B2} is the resistance between base B_2 and the emitter, and the value is fixed.

Consider the circuit as shown in figure 1.

Let $I_E = 0$. Due to the applied voltage V_{BB} a current I results as shown.

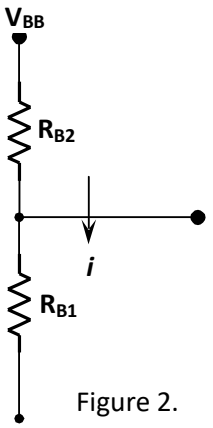


Figure 2.

Form the equivalent circuit, it is evident that the diode cannot conduct unless the emitter voltage

$V_E = V_{\square} + V_1$, *where* $V_{\square}$ *is the cutin voltage of the diode.*

This value of the emitter voltage which makes the diode conduct is termed as ***peak voltage***, and it is denoted as V_P.

We have $V_E = V_{\square} + V_1$,

or since $\boxed{V_P = V_? + ?V_{BB}}$ $V_1 = \square\ V_{BB}$.

It is obvious that if $V_E < V_P$, the UJT is OFF, and

if $V_E < V_P$, the UJT is ON.

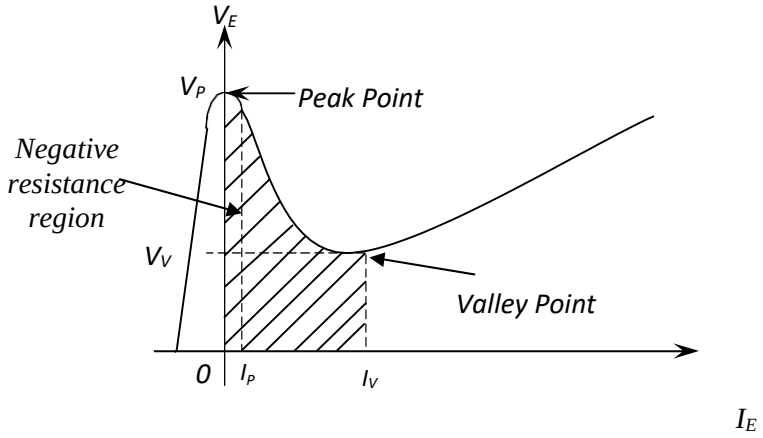


Figure 3.

The main application of UJT is in switching circuits wherein rapid discharging of capacitor is very essential.

Having understood the basic of UJT, we shall next study the working of UJT relaxation oscillator.

Working of UJT relaxation oscillator (OR UJT sweep circuit):

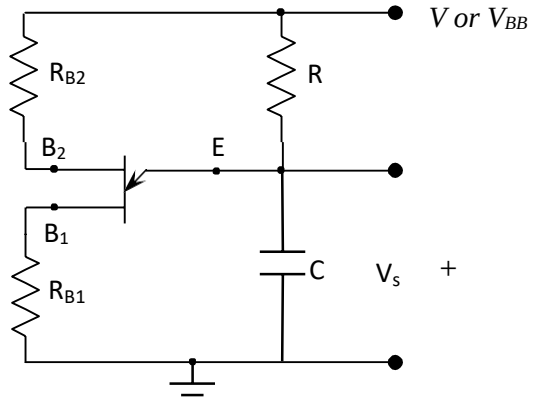


Figure:4

The UJT sweep circuit shown in the figure 4 consists of a UJT, a capacitor and a resistor arranged as shown.

We studied that a UJT is OFF as long as $V_E < V_P$, the peak voltage. Hence initially when the UJT is OFF, the capacitor *C* charges through the resistance *R* from the supply voltage *V*.

Let V_S = capacitor voltage.

It is seen that when the capacitor voltage V_S rises to the value V_P the UJT readily conducts. When the UJT becomes ON, the capacitor discharges and its voltage falls. When the voltage falls to the valley point V_V, the UJT becomes OFF and the capacitor charges again to V_P.

This cycle of charging and discharging of the capacitor *C* repeats, and as a result, a saw tooth wave form of voltage across *C* is generated.

CIRCUIT DIAGRAM :

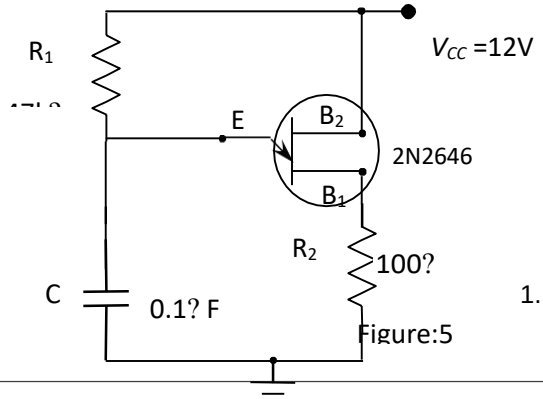
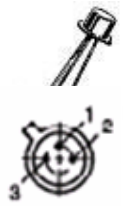


Figure:5

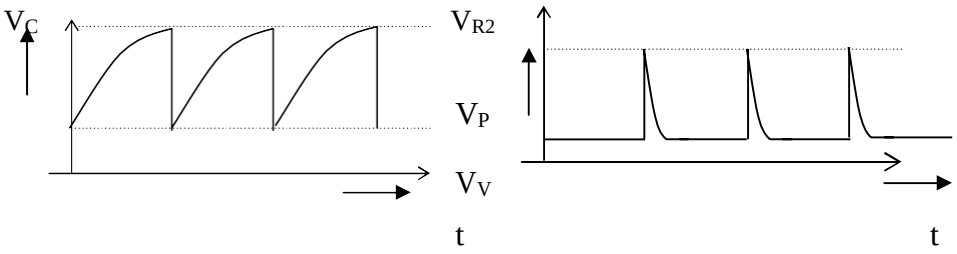


1. Emitter 2. Base1 3. Base2

PROCEDURE:

1. Connect the circuit as shown in figure with designed values.
2. Note down the voltages and frequencies across C& R_2 .
3. The time period of the output wave form is noted and is compared with theoretical value
   $T = R_1 \square C[\ln \{(V_{BB} – V_V) / (V_{BB} – V_P)\}]$
4. Plot the graphs of Vc and $V_{R1.}$

EXPECTED WAVEFORMS:



QUESTIONS:

1. Describe some important applications of a UJT?
2. Is the name UJT appropriate?
3. Write short notes on UJT as a relaxation oscillator?
4. Discuss the concept of –ve resistance?
5. Define the intrinsic stand off ratio and explain its importance?

CONCLUSIONS:

Conclusion can be made on how the UJT works as a saw tooth generator, which components in a UJT circuit is used to generate the saw tooth wave form and also conclude on time period of the output wave form of UJT theoretically and practically and also made on if the output waveform of the UJ are identical with the theoretical wave forms or not.

SINGLE STAGE COMMON SOURCE JFET AMPLIFIER

Objectives:

The objective of this experiment is to calculate theoretically and verify experimentally the following performance parameters of a given JFET Amplifier.

1. The DC Operating Point.
2. The maximum signal handling capacity of the amplifier, without distortion.
3. The output impedance of the amplifier.
4. The gain frequency response of the amplifier.

Pre lab:

1. Study the data sheet of JFET BFW10/11 and note the following :
   a. The type of JFET
   b. The pin or base diagram of the JFET
   c. The maximum rating of V_{DS}, V_{GS}, P_D, and T_j
   d. Values of I_{DSS} and V_{PO}
   e. Typical values of r_{ds} and g_m.
2. Study the effect of the temperature changes on the operating point of a JFET and the need for the stability of the DC operating point.
3. Explain different types of JFET biasing schemes and compare them.
4. Calculate the DC operating point I_{DSQ} and V_{DSQ} of the Amplifier circuit in fig 9.1(a).
5. Calculate g_m of the JFET, at the Operating point calculated in step 4.
6. Draw the AC and DC load lines for the circuit in Fig.9.1(b) and estimate the maximum un-distorted peak to peak output signal amplitude.
7. Calculate the mid-band voltage gain of the amplifier.
8. Calculate the mid-band output impedance of the amplifier.
9. Sketch the Gain-Frequency plot of the amplifier.

Components and Equipment:

Resistors : carbon, ¼ watt and 5% -600Ω, 3K, 10K, 30K, and 150K - one each Capacitors: Electrolytic - 100µF, 25V 1 No and 10 µF, 25V 2 No's.

FET : JFET BFW10/11 - 1No

Wires and cables – as

required DMM - 1 No.

Function generator -1 No.

DC power supply – 0-30V, 1A – 1No.

Circuit Diagram:

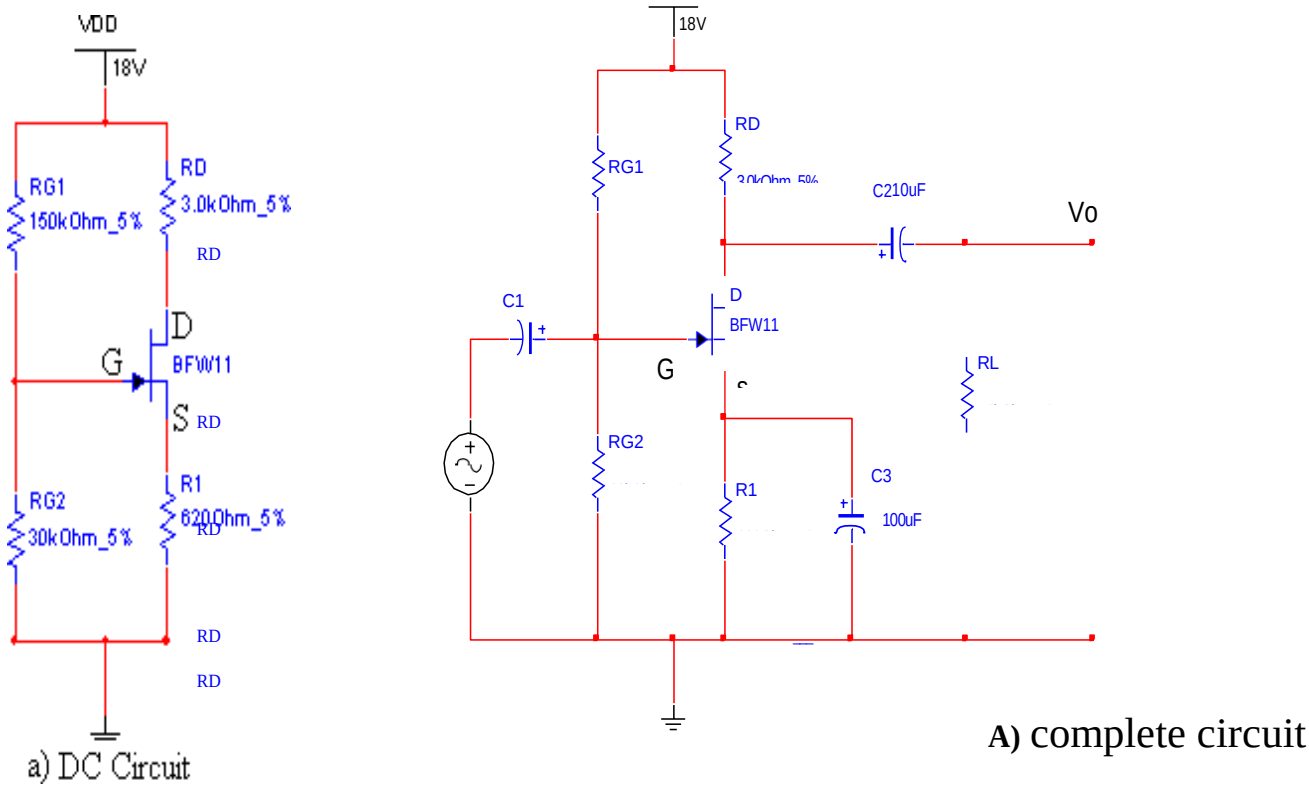


Fig 9.1 Single Stage Common Source JFET Amplifier

Procedure:

DC Operating Point:

1. Connect the circuit in Fig 9.1(a)
2. Measure V_{GSQ} and V_{DSQ}
3. Measure the Voltage across R_D and calculate I_{DSQ}
4. Compare V_{GSQ} & I_{DSQ} with the theoretically calculated values.

Maximum Un-distorted output signal:

1. Connect the circuit in Fig.9.1(b) and fix the frequency of the function generator at 5 KHZ
2. Connect the CRO at the output of the amplifier.
3. Increase the signal input to the Amplifier and observe the amplifier output waveform on the CRO. Increase the input until the output exhibits distortion and record the peak values

   V_{smax} V_{imax} and V_{omax}

Output Impedance:

4. Adjust the input signal amplitude to a value below V_{smax} in step 7
5. Measure and note V_s, and V_o.
6. Measure and note V_s, and V_{oNL} without R_L or 10K.
7. Calculate $R_o = [(V_{oNL}-V_o)/V_o]*R_L$.

Gain –Frequency Response:

8. Connect R_L and adjust the input signal amplitude to 50mv peak to peak.
9. Vary the input sine wave frequency from 10HZ to 1 MHZ in suitable steps and measure the output Voltage V_o at each step; using CRO. Make sure the input voltage ,Vs, is kept constant throughout the frequency range.

Record the readings in the tabular column as shown.

Vs= 50mvp-p constant, V_i =

Frequency (f)	V_o(p-p)	$A_v=(V_o/V_i)$	Gain in dB =20log $_{10}A_v$
10Hz …… ……. ……. . 1 MHz			

Post – lab:

1. Compare experimentally obtained operating point, mid-band gain, maximum undistorted signal and the output impedance with the theoretically calculated values. Explain the discrepancies.
2. Plot the graph gain A_v vs frequency (f) on a semi-log graph paper.
3. Calculate the bandwidth of the amplifier; marking the frequency points, where the gain reduces to 0.707 of its maximum value.

Questions:

1. Why the gain reduces or falls at lower and higher frequencies.
2. Compare the BJT Common Emitter and FET Common Source amplifiers.